Claimsims

[c1] A method of processing memory reads and writes in a packet processor comprising the steps of: processing memory reads having an associated sequence number; processing memory writes having an associated sequence number; signaling a restart of a particular sequence numbers when a memory conflict is detected.

[c2] The method of claim 1 wherein the step of processing memory reads comprises the steps of: recording the address and sequence number in a read table; searching a write table for an entry with a matching address and a sequence number equal to or less than the received read; upon detecting a match, retrieving data from the write table.

[c3] The method of claim 2 wherein the step of processing memory writes comprises the steps of: recording the write address, write sequence number and write data in a write table; searching a read table for an entry with a matching address and a sequence number greater than the received memory write.

[c4] The method of claim 3 further comprising the step of: processing a start signal with an associated sequence number and a done signal with an associated sequence number to maintain a list of active sequence numbers.

[c5] The method of claim 4 further comprising the steps of: sending write data to a memory system upon receipt of said done signal; flushing the entries in said read table and said write table corresponding to said sequence number associated with said done signal.